**ABSTRACT**

Artificial Intelligence is based on many things like Mathematical equations and artificial neurons. The main focus of this neural architecture is the implementation of a chip layout design and its trained using Power Gating (PG) Technique in an analog domain with a new technique of producing power to the CMOS board using VLSI application. The Analog components used are Gilbert Cell Multiplier (GCM), Neuron Activation Function (NAF) and Adders for the implementation. The Existing system consumes designing of Signal Compression and Decompression using Back Propagation (BP) Algorithm of Neural Network (NN).Back Propagation uses a digital computer to calculate weights when the final network is hardware and it loses its plasticity. Moreover the calculation is slow and training speed is slow. The Power consumption is high and overall delay is also high. Compression and Decompression done in lossy data not in lossless data. The Proposed system comprises of Power Gating Technique and this reduces power and thus overcomes the disadvantage of the existing system. Signal Compression and Decompression are designed using Power Gating Technique. Layout Design and is Verification of the Power Gating Technique carried out Using Micro wind 2.6 (Back-End tool).The Technology used in the designing layout is 0.12 Micrometer Technology.